REMARKS

Claims 1-18 are pending in the application.

A new title of the invention has been submitted herein.

It should be noted that the Abstract of the Disclosure submitted in applicant's amendment contains less than 150 words.

The Examiner's objections to the claims as well as his rejection of claim 1 under 35 U.S.C. 112, second paragraph have been overcome in the amended claims. Reference numerals have been included in some claims to clarify claimed subject matter.

Claims 1 and 5-11 are now rejected under 35 U.S.C. §103 as being unpatentable over Shiell (5,864,697) in view of Shintani (4,532,589) further in view of Nakanishi (5,835,754) and further in view of Hara (5,740,415. The Examiner admitted that Shiell fails to disclose an instruction buffering portion with a plurality of instructions buffers and a branch target address information buffer portion.

Claim 12 is rejected under 35 U.S.C. §102 as being anticipated by Shiell (5,864,697).

Claims 2-4 are again rejected under 35 U.S.C. §103 as being unpatentable over Shiell in view of Shintani et al, and further in view of Nakanishi.

Claims 13 and 14 are rejected under 35 U.S.C. §103 as being unpatentable over Shiell, Shintani and further in view of Lee et al. article.

Claims 15-18 are rejected under 35 U.S.C. §103 as being unpatentable over Shiell in view of Lee et al.

Independent claims 1, 2, 6, 12 and 16 have been herein amended to more clearly define the claimed invention over the art.

Regarding the rejection of claims 1 and 5-11 the Examiner admitted that Shiell does not teach an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from the instruction store portion. The Examiner further admits that Shiell in view of Shintani fails to teach a branch target address information buffering portion including at least first and second branch target address information buffers which, when the branching instruction detection portion has detected a branching instruction, buffer the branch target address information fo9r generating the branch target address of that branching instruction but Nakashini, in the Examiner's opinion does teach the above concept.

In Nakanishi, the double BTB structure for a super-scalar processor is disclosed. Before discussing Nakanishi, the function of BTB disclosed in Nakanishi should be explained. When a processor executes an instruction with pipeline processing, an instruction should be pre-fetched before executing the preceding instruction. In order to pre-fetch a branch target side instruction, however, the branching instruction should be executed and the branch target address should be calculated based on the execution result. This means that the pre-fetching of the branch target side instruction can not be possible. Therefore, when the processor executes a branching instruction and calculates the branch target address, such branching instruction and the calculated branch target address is stored in the BTB. Therefore, the BTB accumulates a large number of branching instructions and the branch target address thereof. Then, when the branching instruction is pre-fetched by the instruction address, BTB is also accessed by the instruction address so that the branch target address can be obtained without executing the branching instruction. This enables the pipeline processing.

In Nakanishi, since the super-scalar processor fetches plural instructions simultaneously, the double BTB are provided so that the branch target address for the plural instructions can be

detected from the double BTB. Therefore, in Nakanishi, the branch target address is selected based on the fetch address from a large number of entry (branch address) in BTB.

On the other hand, in the present invention recited in claim 1 and 2 also in claim 2, as amended the first or the second branch target address information buffer is selected based on the execution result of the first branching instruction, not based on the instruction fetch address. Thus, the first and second branch target address information buffers are totally different in structure and function from the BTB disclosed in Nakanishi.

The same amendments are applied regarding the rejection of claims 2-4 rejected under 35 U.S.C. 103 as being unpatentable over Shiell in view of Shintani et al and further in view of Nakanishi.

Hara (5,740,415) teaches an instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy, which has a branch execution unit, to process data from an instruction decoder with branch instruction information read from a branch target buffer.

Lee also fails to suggest the present invention as claimed in claim 12 from which claims 13 and 14 depend, as well as of claim 16 upon which claims 17-18 depend.

Hara, even if combined with Shiell, Shintani and Nakanishi would fail to teach a skilled artisan the present invention as recited in independent claims 1, 2 and 6 as amended because there is no motivation nor suggestion in any of the cited references to modify or combine them as suggested by the Examiner.

It is well-established that a combination of limitations, some of which separately may be known, may be a new combination of limitations which is not obvious under the condition of 35 U.S.C. §103. Moreover, "an examiner may often find every element of a

claimed invention in the prior art." In re Rouffet, 47 USPQ3d 1453, 1457 (Fed. Cir. 1998) (reversing PTO obviousness rejection based on lack of suggestion or motivation to combine reference).

Therefore even if every element of a claimed invention is in the combined prior art there must be some suggestion or motivation to combine the references. "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form must nevertheless be clear and particularity." In re Dembiscak, 175 F.3d 994, 999 (CAFC 1999).

With respect to the rejection of claims 12 and 16, Shiell does not perform the main memory access, after cache miss based on a branching prediction of the branching instruction as in claim 12 or based on the branch direction being determined as in claim 16. As explained above, the BTB is accessed simultaneously when an instruction is fetched, so that the branch target address can be obtained from BTB without executing the fetched instruction. And either the sequential side instruction or the target side instruction is fetched based on the output from BTB. Therefore, once the instruction fetch is started, the main memory access is performed every time when the cache miss has occurred.

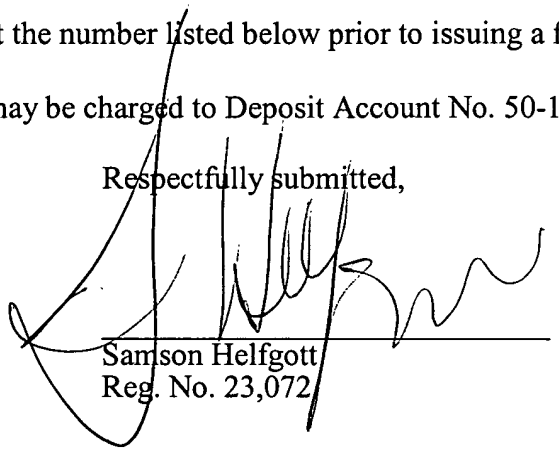
On the other hand, in the present invention as claimed in claims 12 and 16, both of the sequential side instructions and the target side instruction are pre-fetched in spite of the branch prediction. And once the cache miss has occurred while pre-fetching the instruction, the main memory access is performed based on the branch prediction (claim 12) or based on whether the branching direction of the branching instruction is determined or not (claim 16). In Shiell, the main memory access after cache miss is always performed regardless of the branch prediction, or regardless of the branching direction being determined or not.

Accordingly it is believed that independent claims 1, 2, 6, 12 and 16 are patentably distinguishable and therefore these claims as well as claims 3-5, 7-11, 13-15 and 17, respectively dependent thereupon should be allowed.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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